

Fig. 1

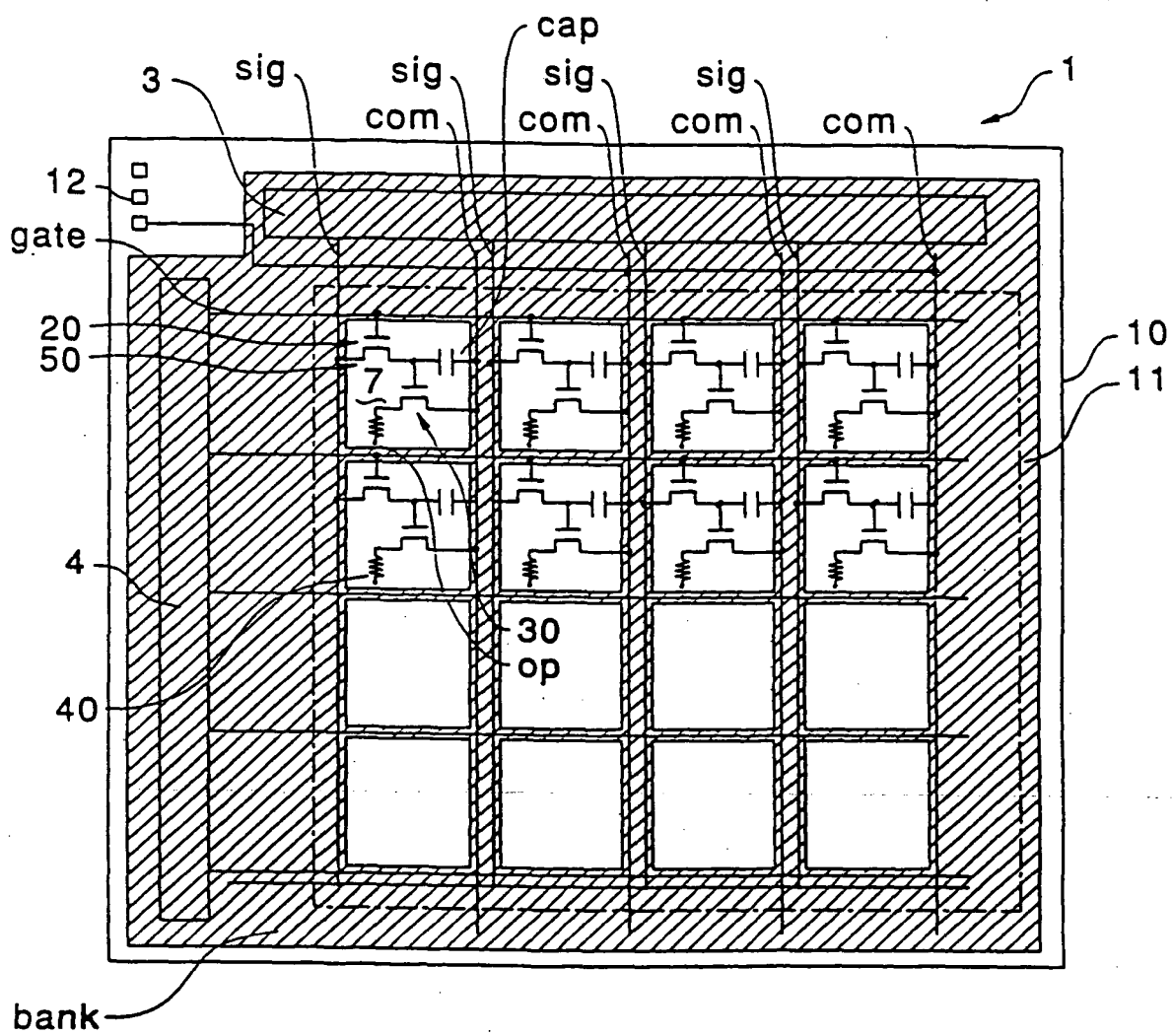


Fig. 2

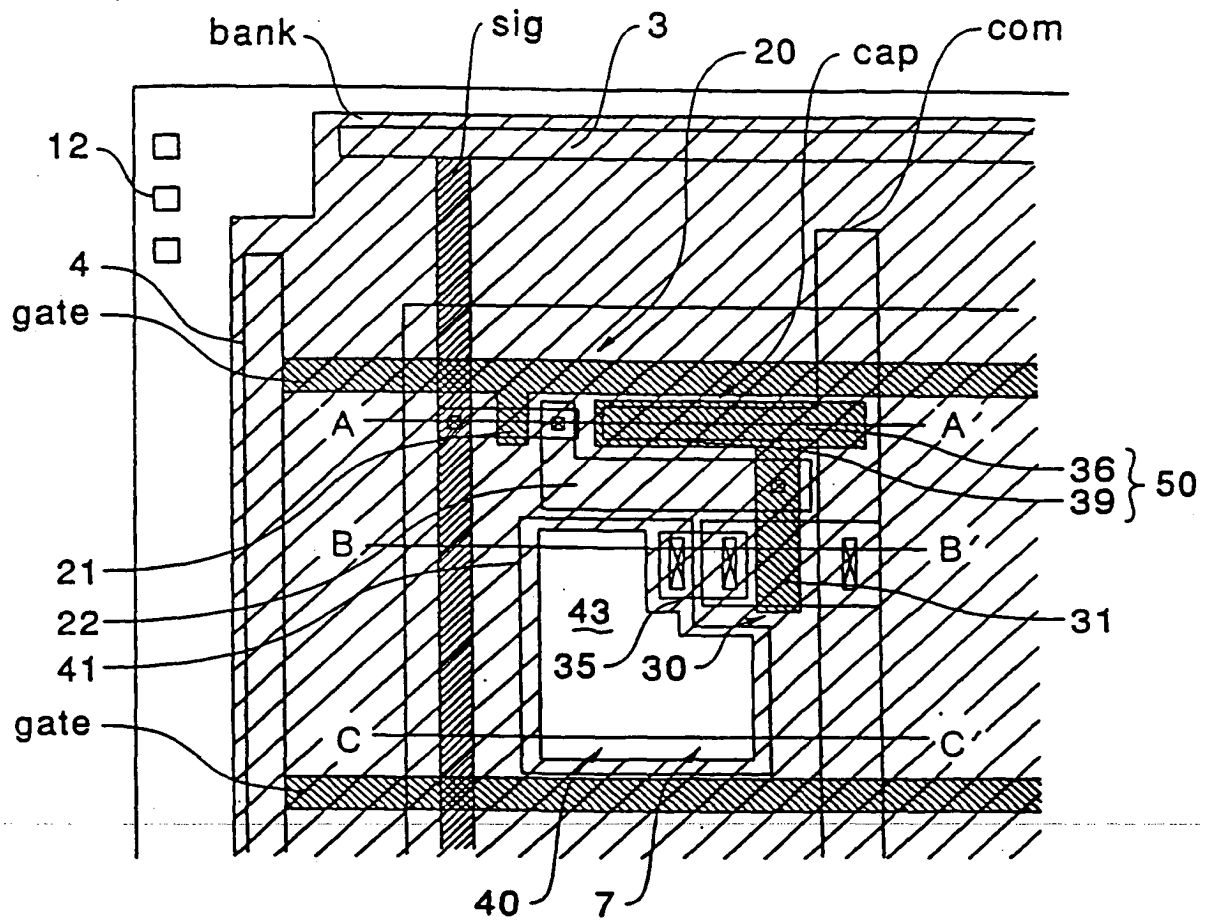


Fig. 3A

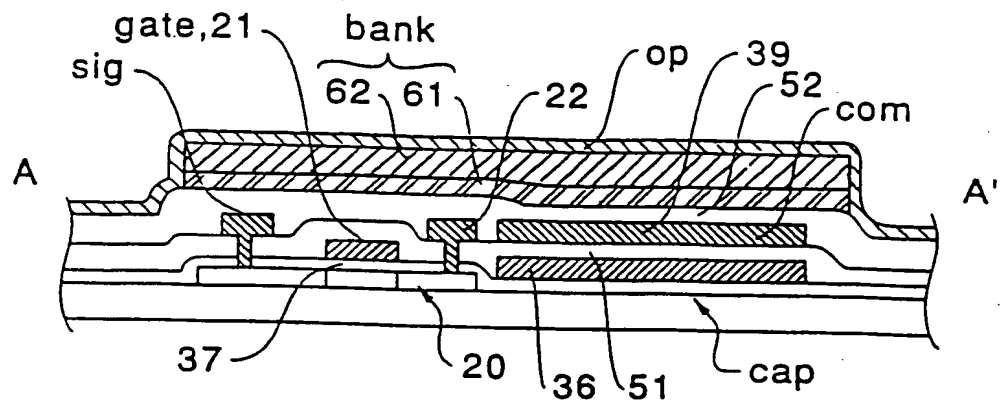


Fig. 3B

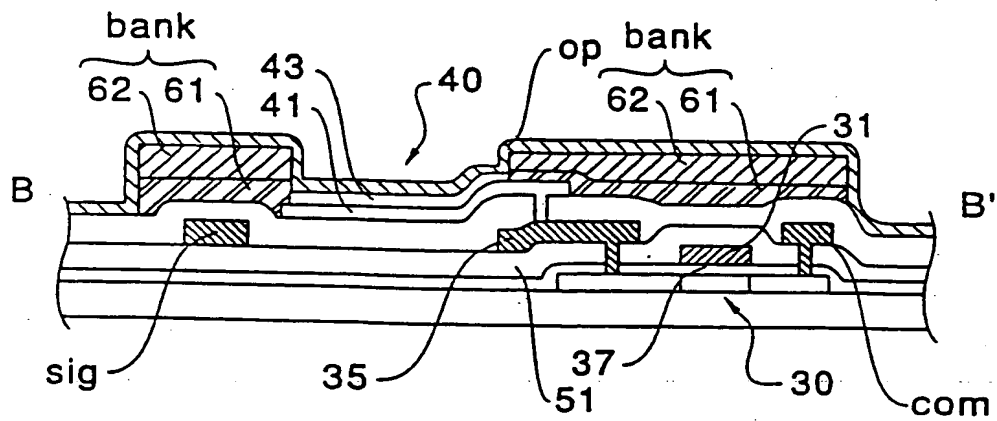


Fig. 3C

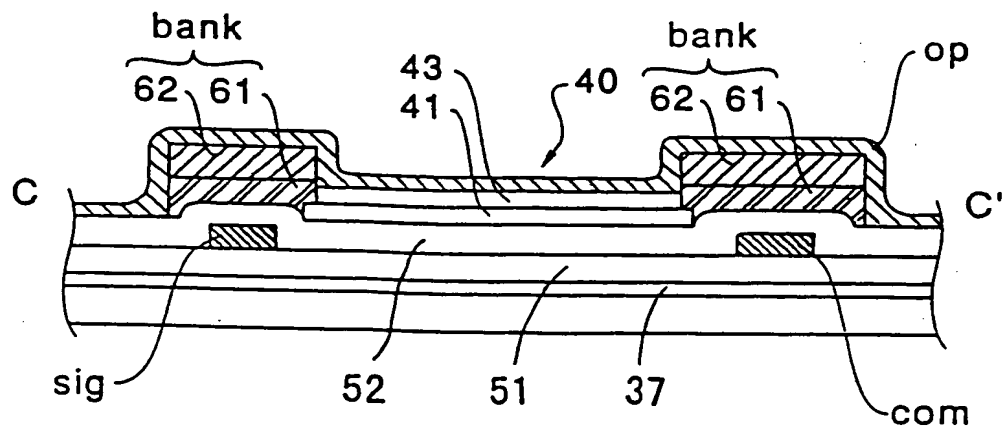


Fig. 4A

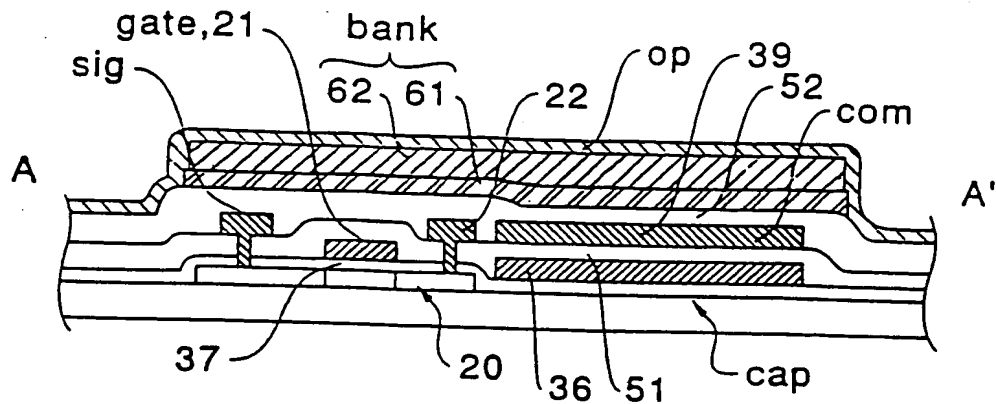


Fig. 4B

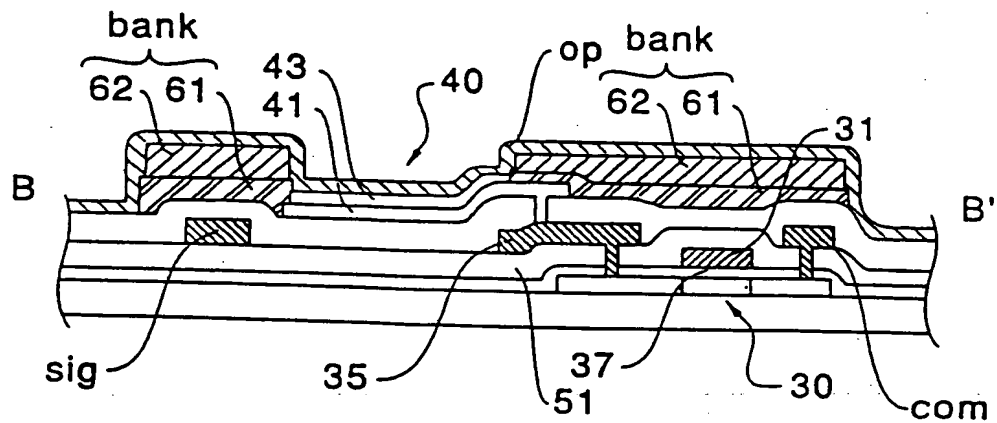


Fig. 4C

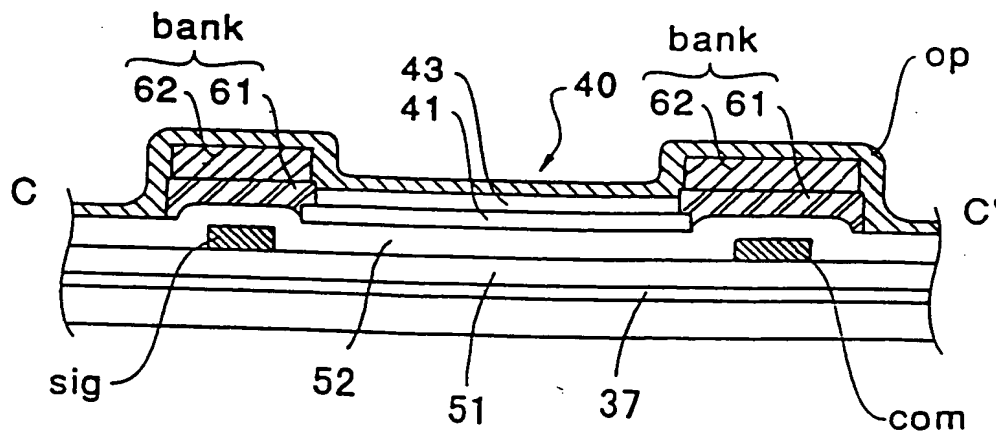
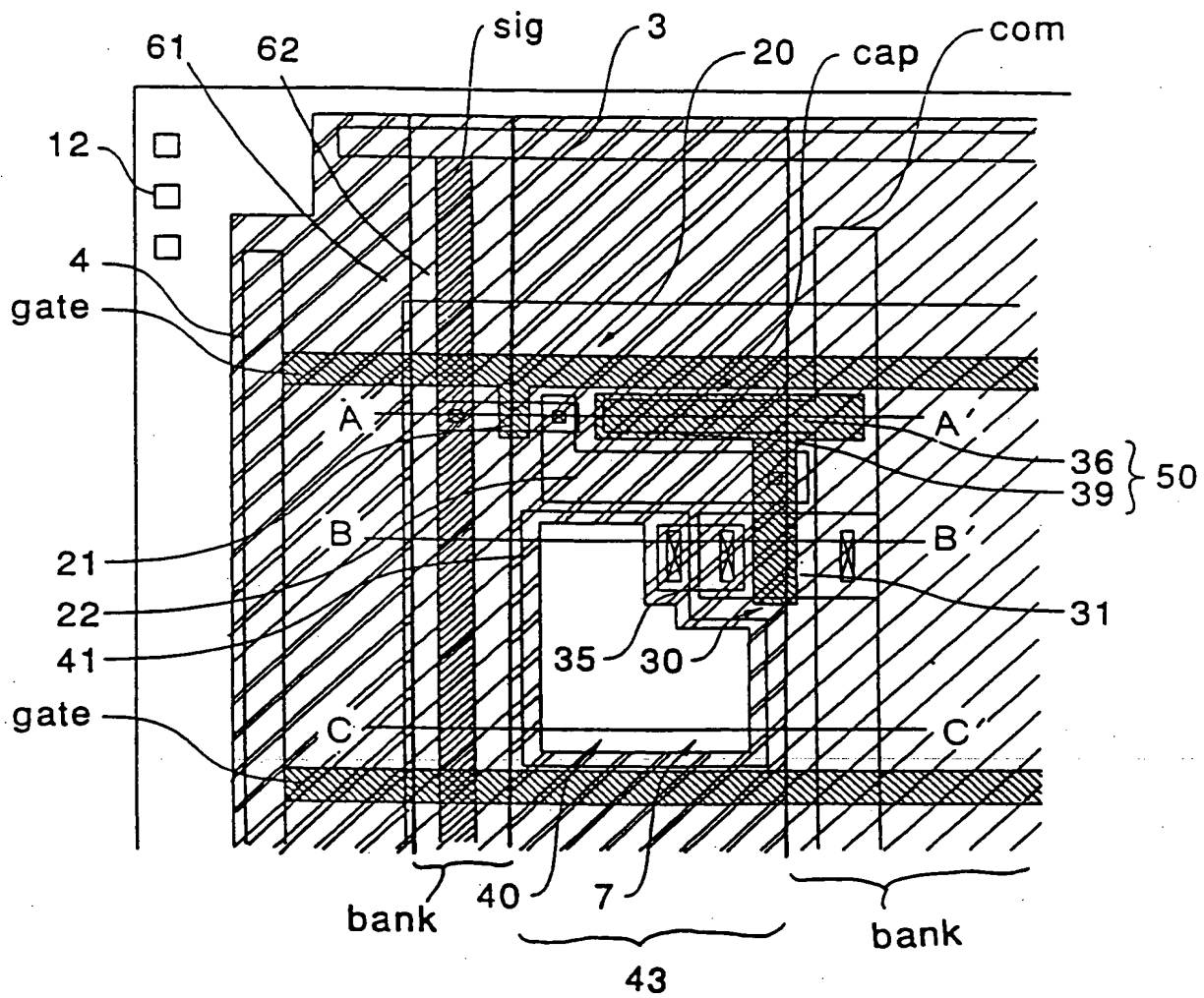


Fig. 5



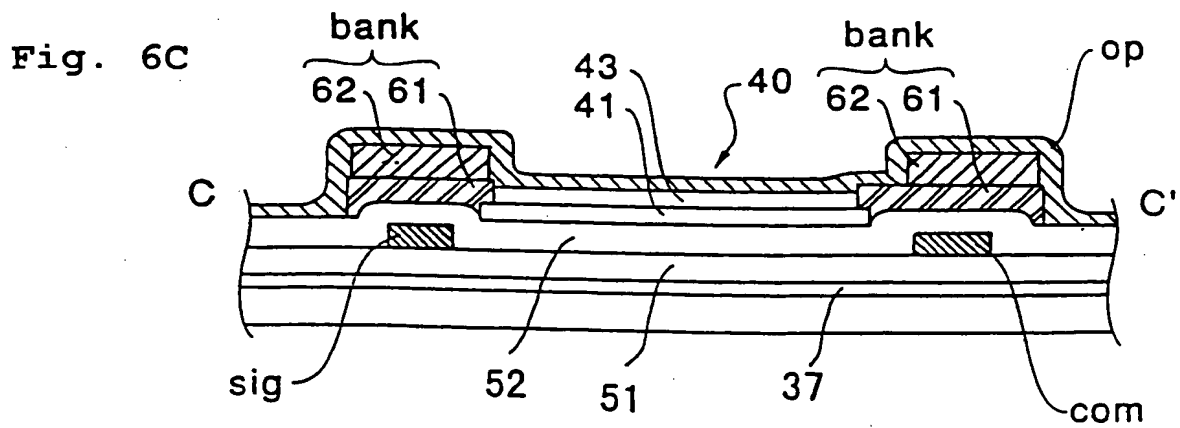
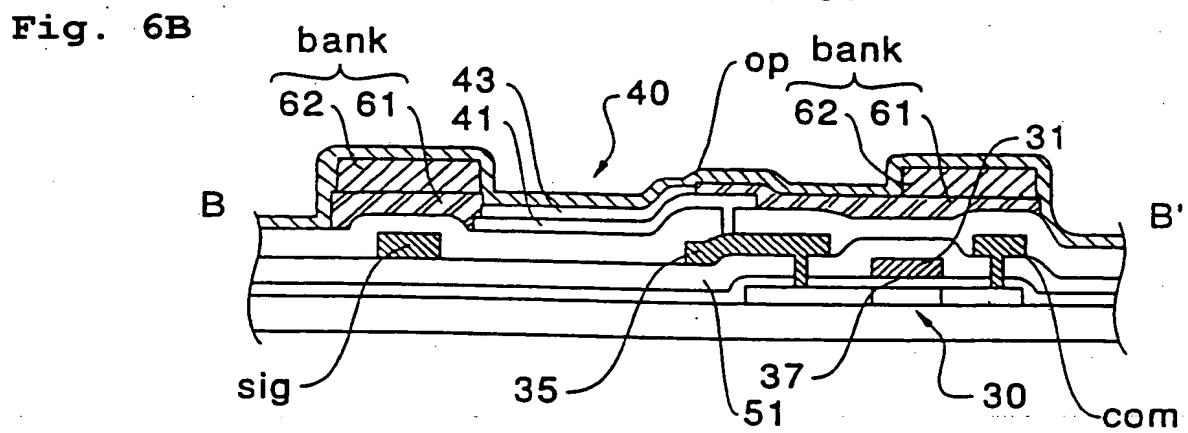
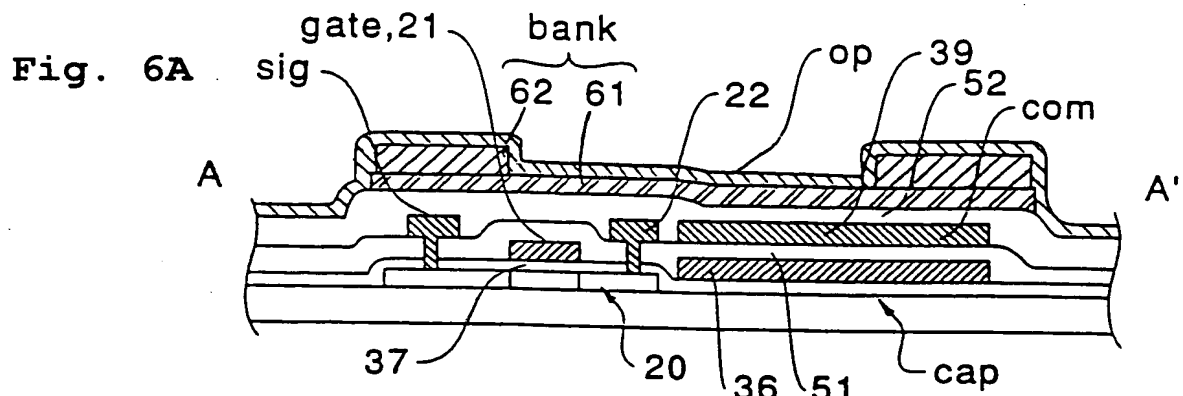


Fig. 7

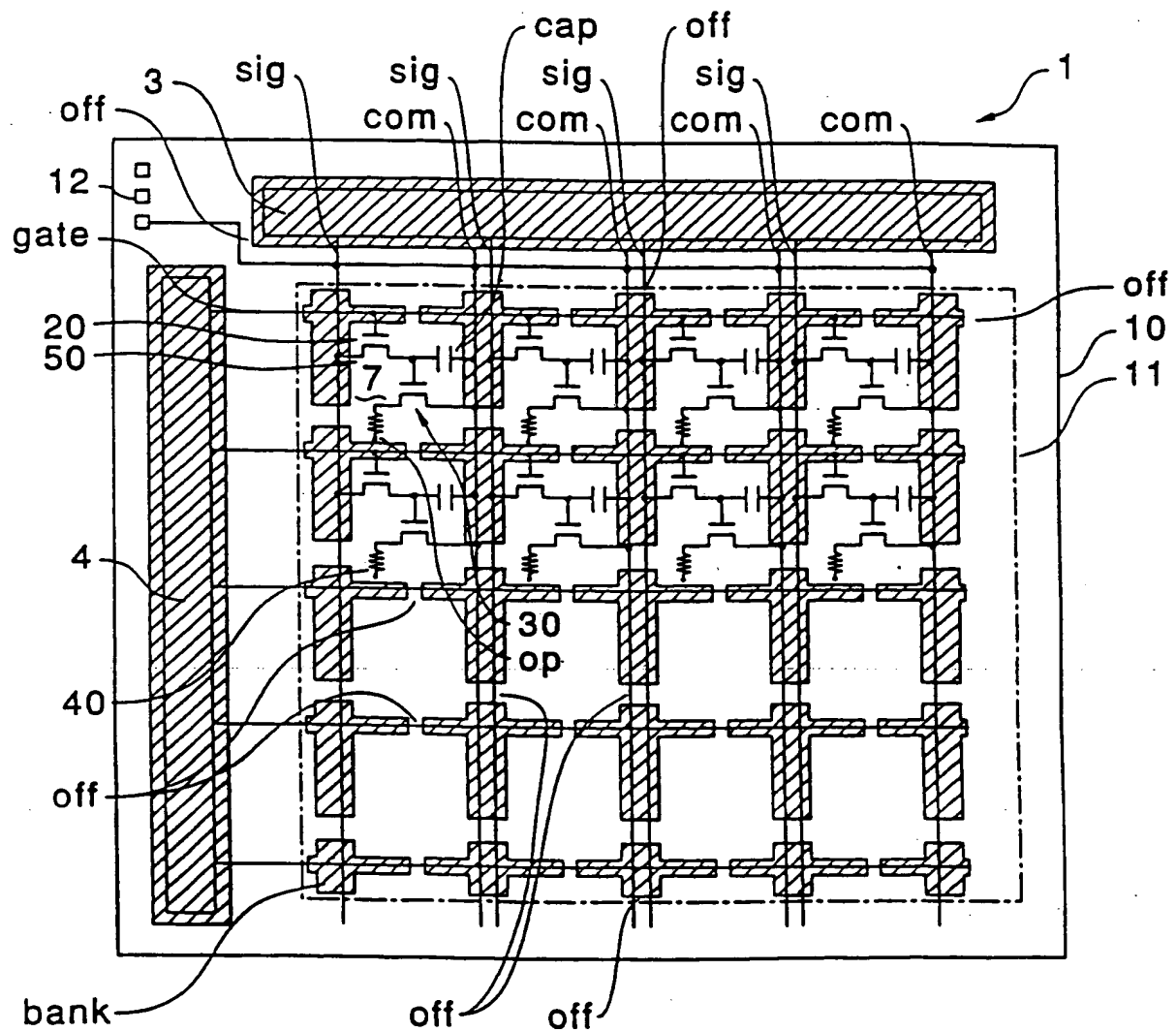
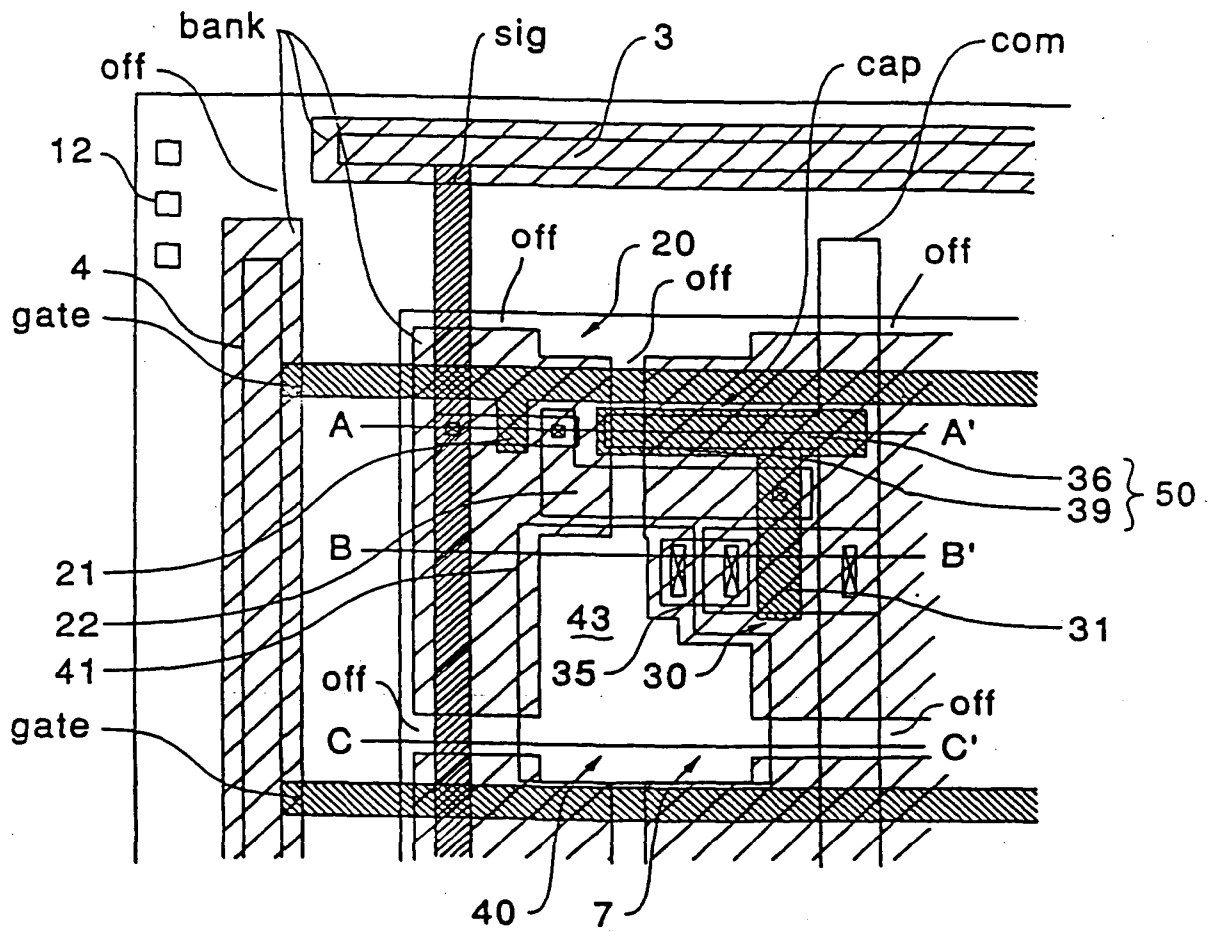


Fig. 8



A cross-sectional view of a semiconductor device, labeled A and A' at the ends. The device features a gate structure (21) and a bank structure (62, 61). Other labeled components include sig, 22, off, op, 39, 62, 61, com, 52, 37, 20, 36, 51, and cap. The diagram illustrates the layered construction and electrical connections of the device.

This diagram shows a cross-sectional view of a semiconductor device with two banks, labeled 'bank' and 'op bank'. The device includes a substrate with a central channel region (30) and side regions (31). The channel region contains a series of gates (35) and a source/drain region (37). The side regions contain a series of gates (31) and a source/drain region (37). The banks are formed on the side regions and contain a series of gates (61, 62) and a source/drain region (41, 43). The device is labeled with 'B' and 'B'' at the ends, indicating a cross-section through the device.

A cross-sectional view of a semiconductor device. A central channel (40) is formed in a substrate (37). The channel is bounded by a top layer (41) and a bottom layer (51). The top layer (41) is covered by a passivation layer (43). The bottom layer (51) is covered by a contact layer (52). The device is terminated at both ends by a contact layer (52) and a passivation layer (43). The ends are labeled C and C'. The device is labeled with various components: 43 (top passivation), 41 (top channel layer), 40 (central channel), op (opening), 52 (contact layer), off (offset), sig (signal), 37 (substrate), 51 (bottom channel layer), and com (common).

Fig. 10

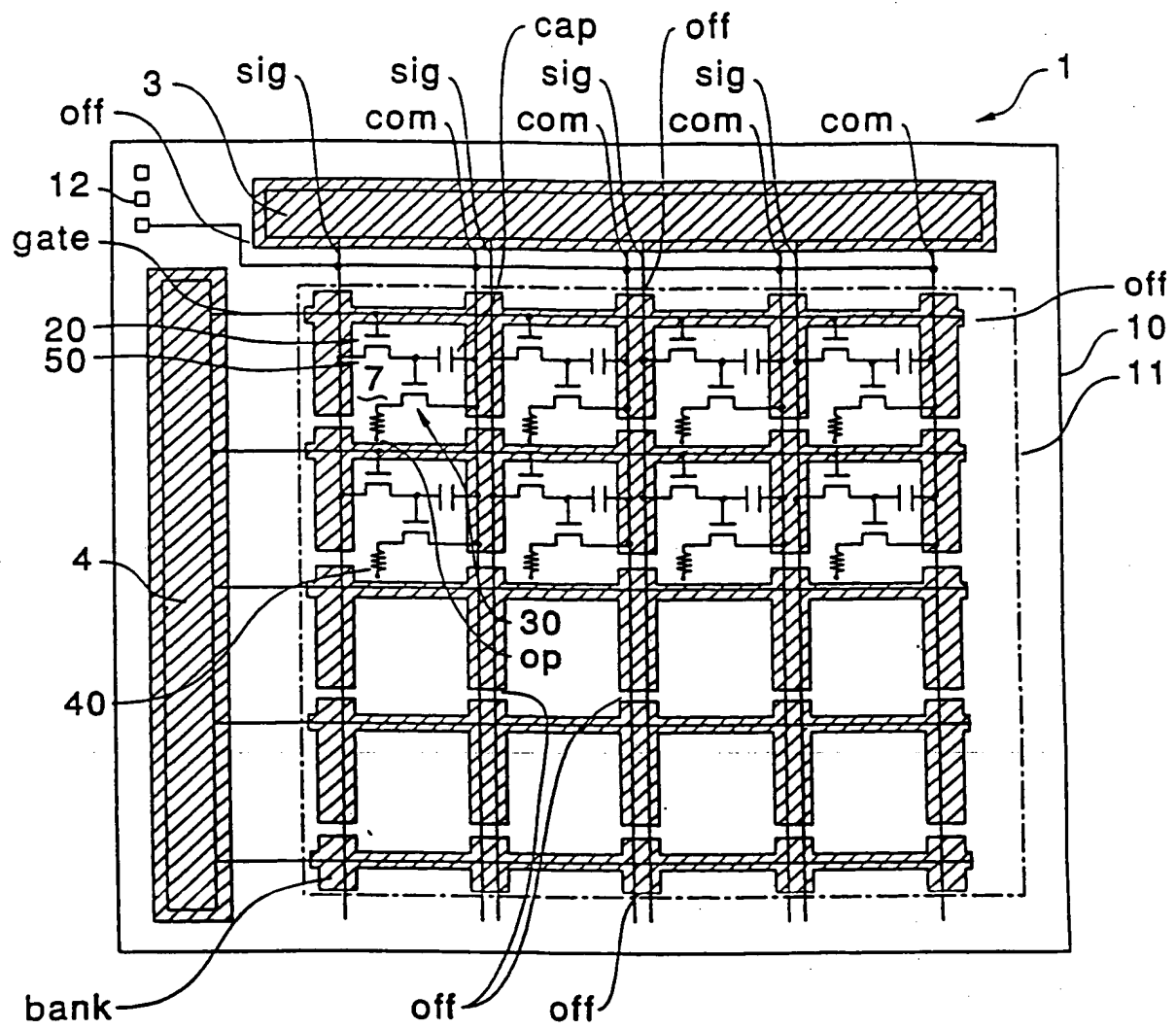
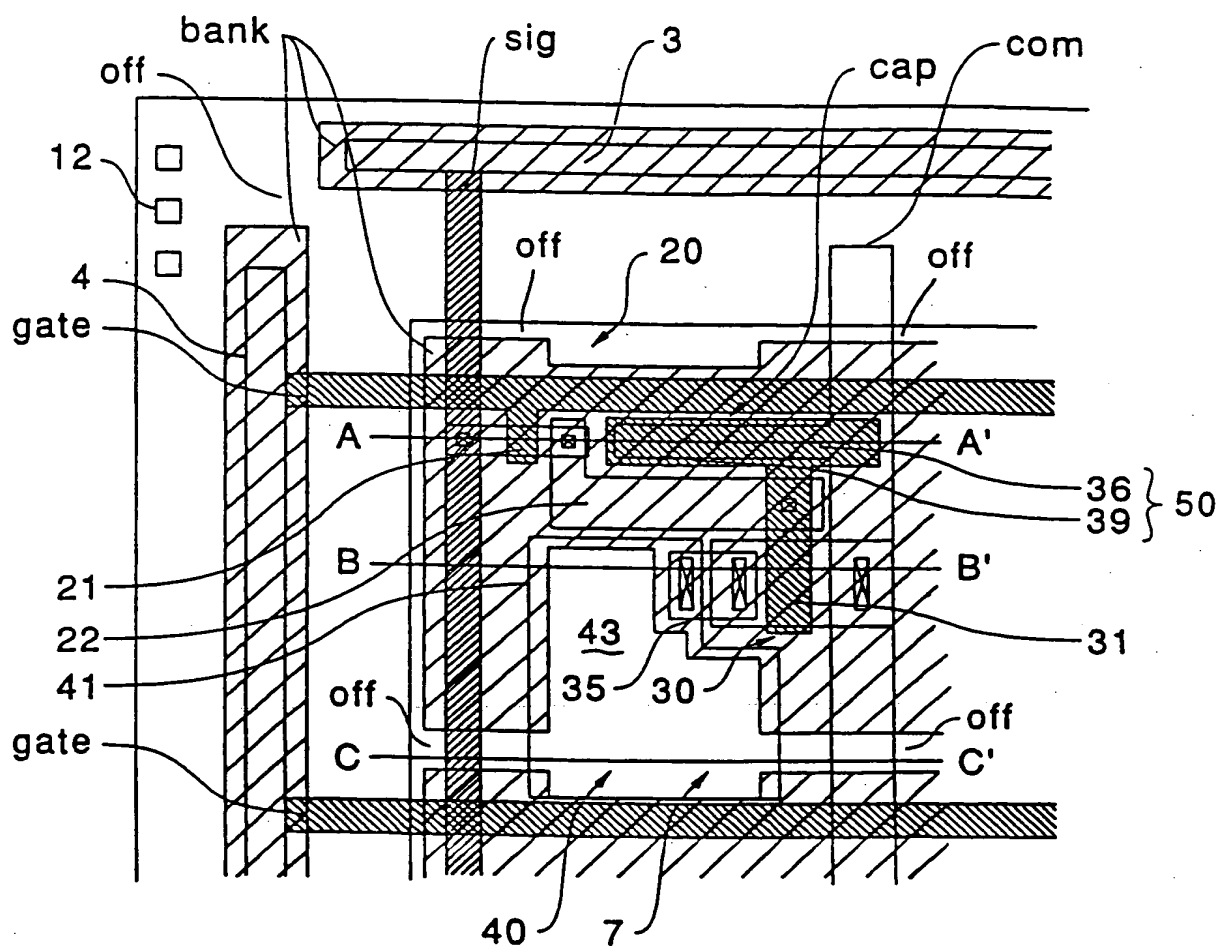


Fig. 11



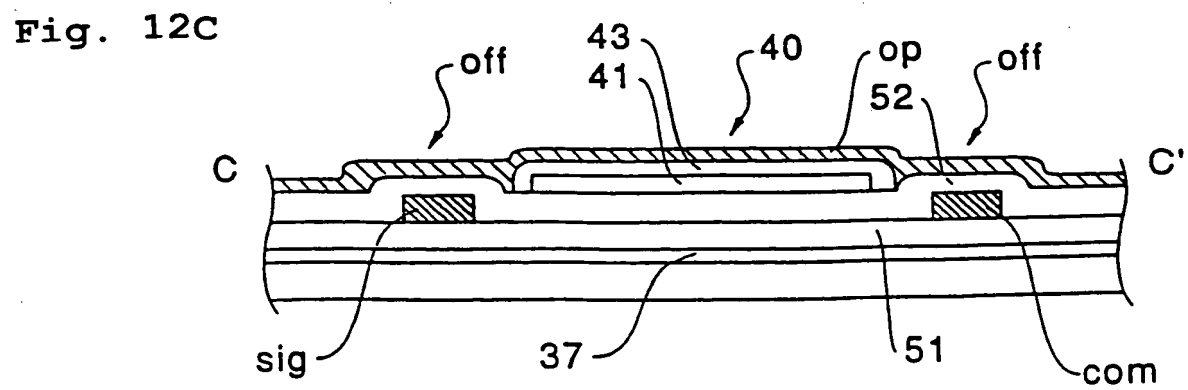
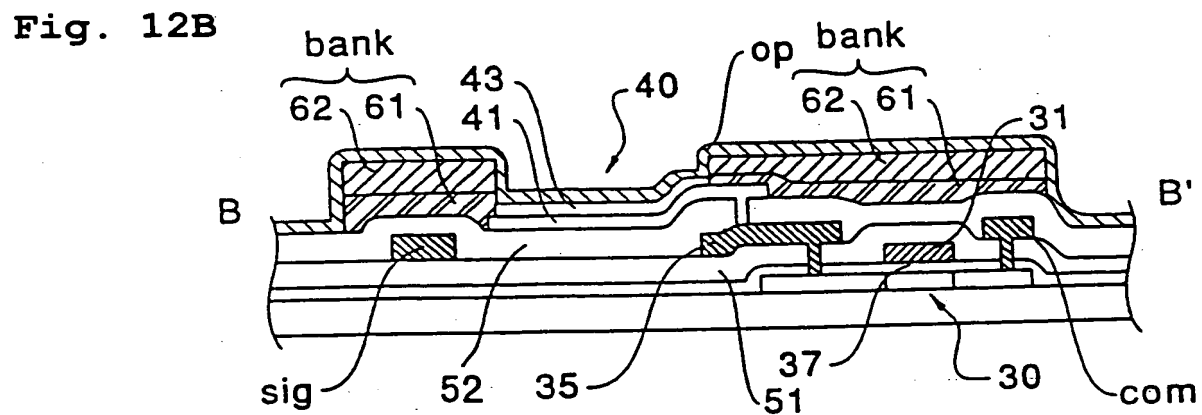
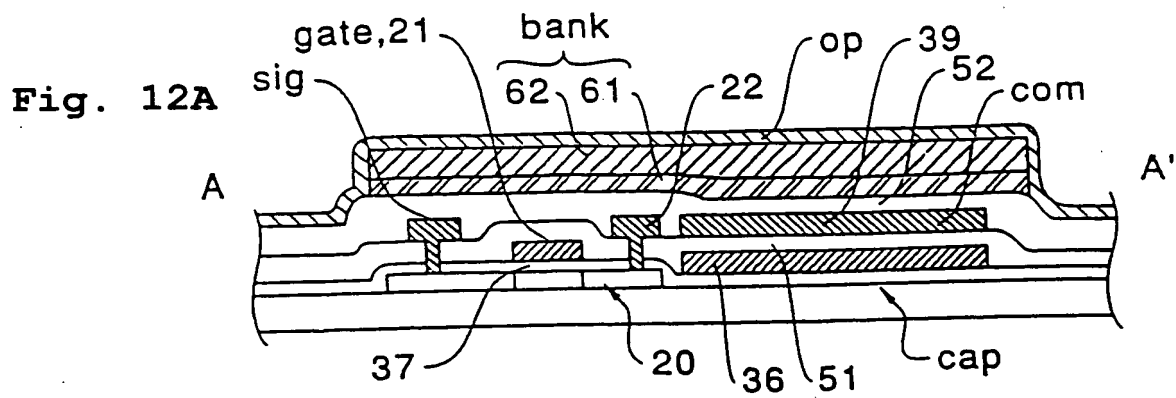


Fig. 13.

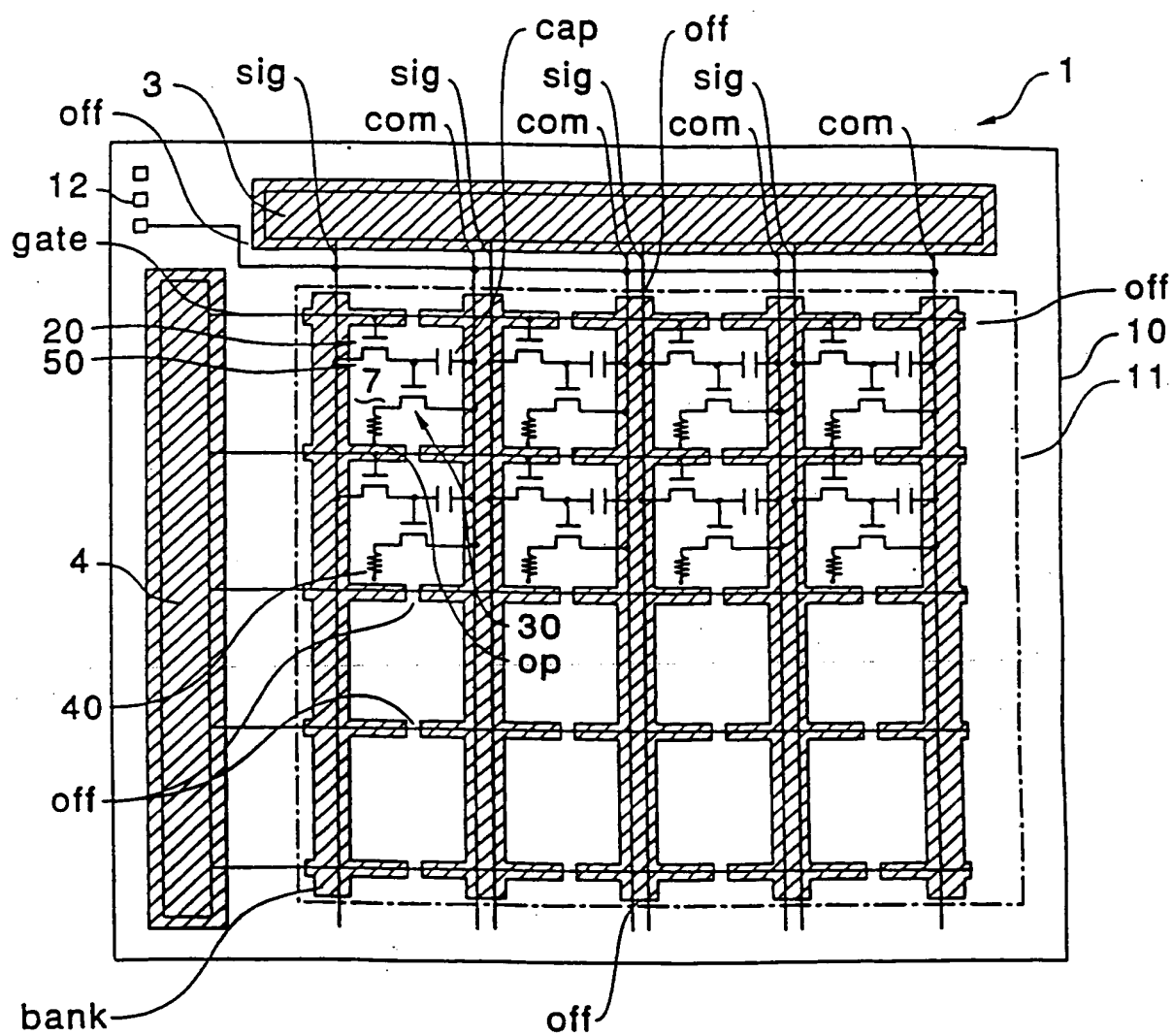


Fig. 14

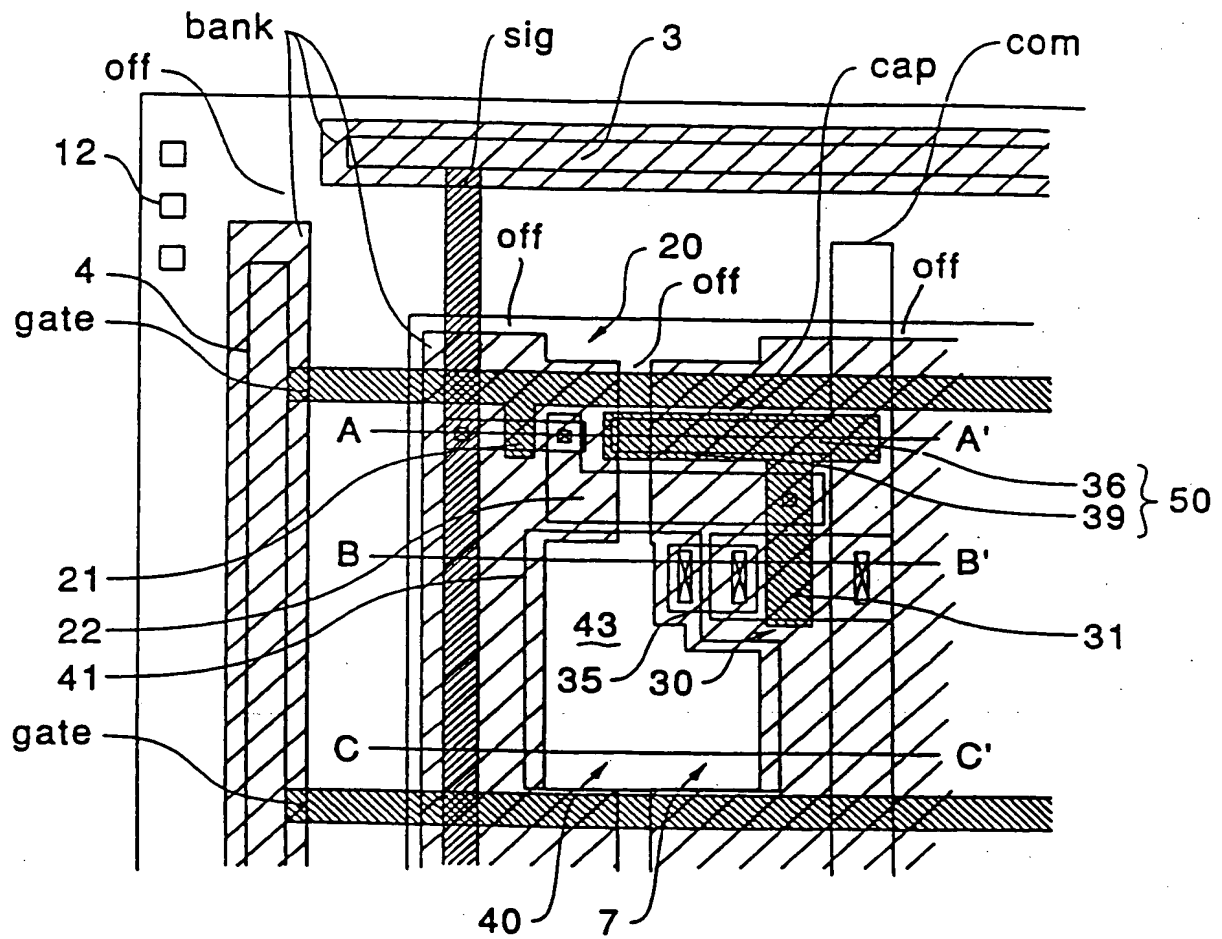


Fig. 15A

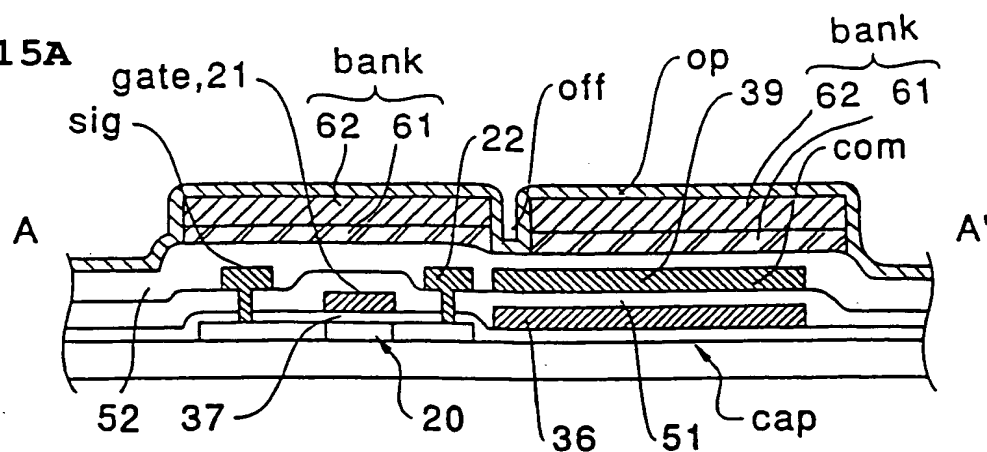


Fig. 15B

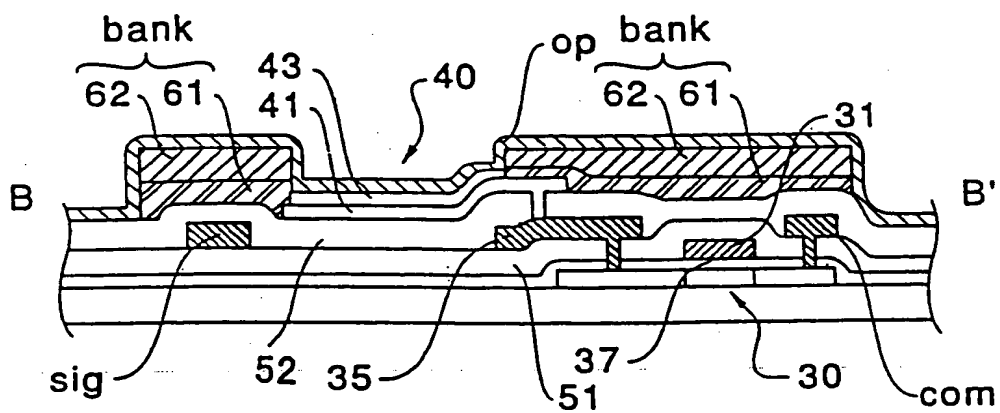


Fig. 15C

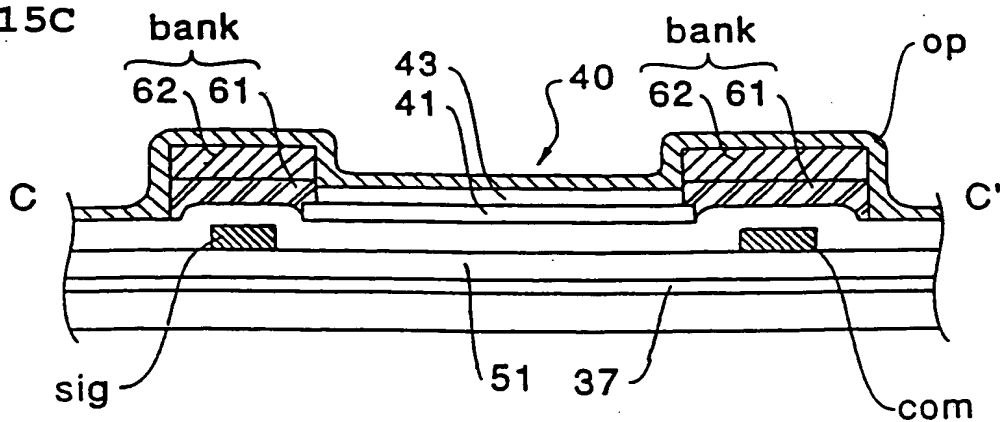


Fig. 16

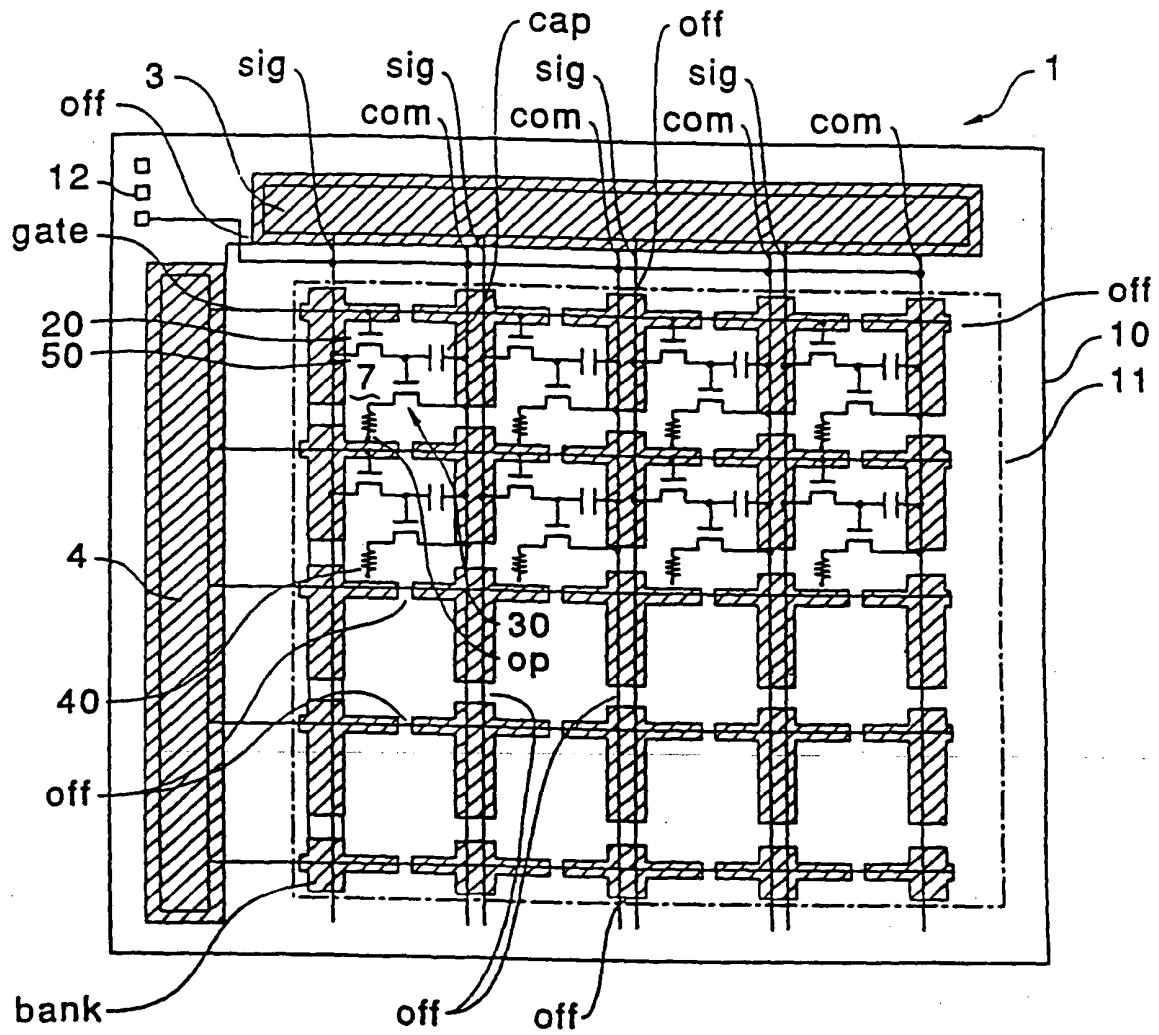


Fig. 17

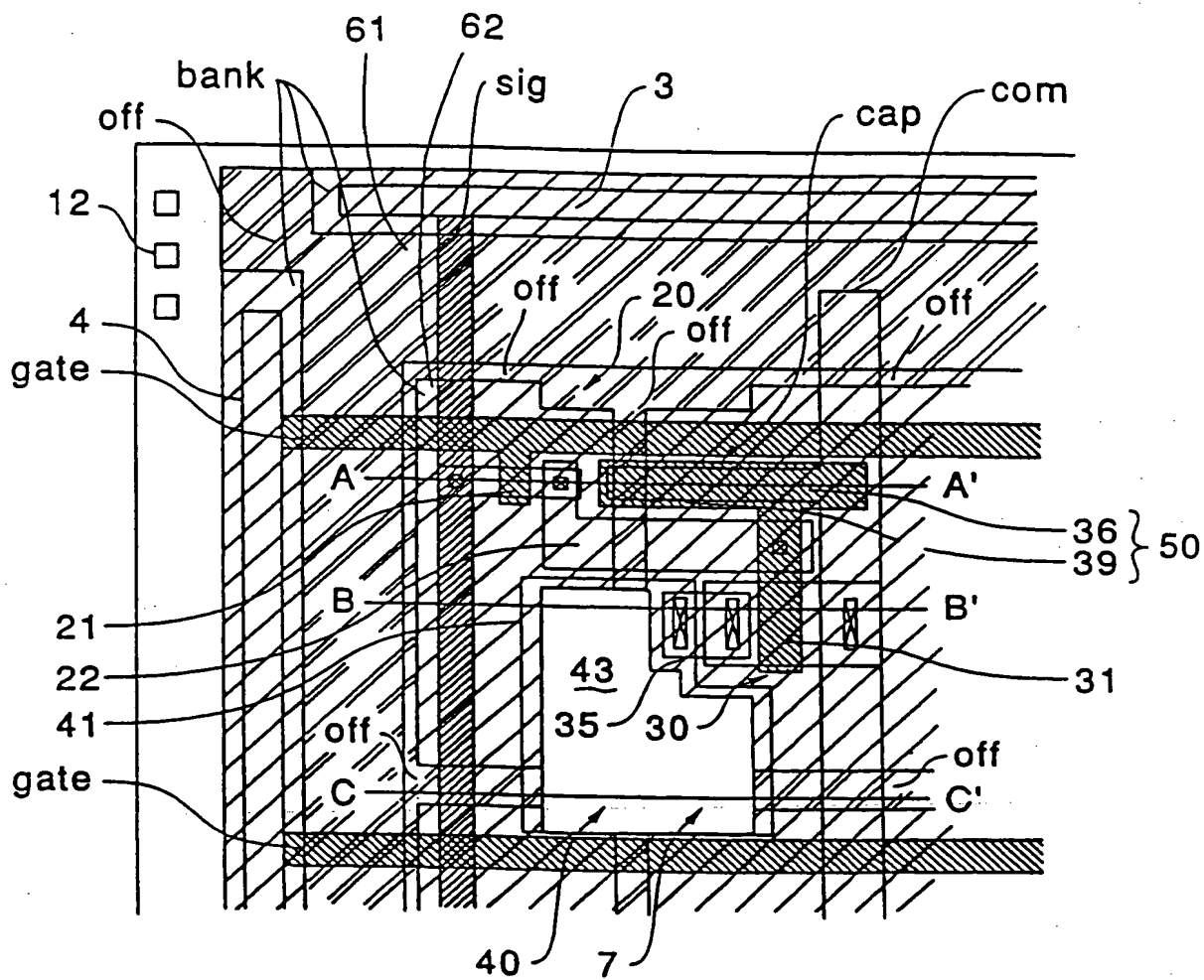


Fig. 18A

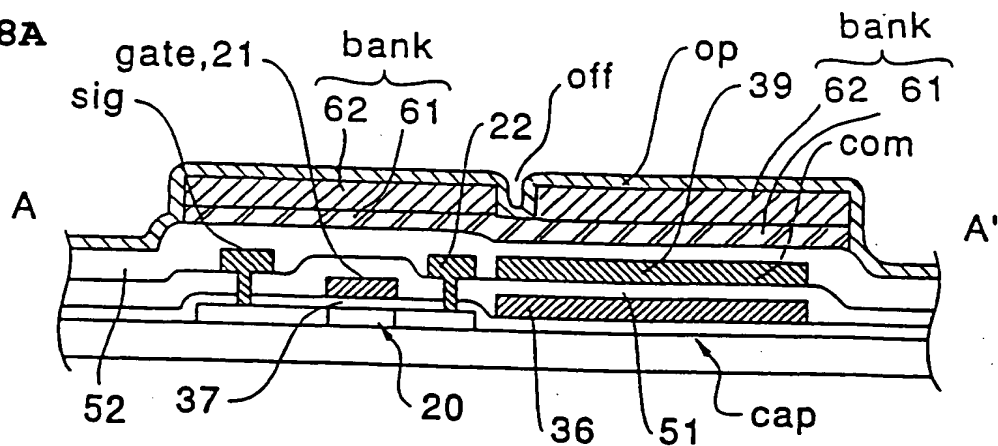


Fig. 18B

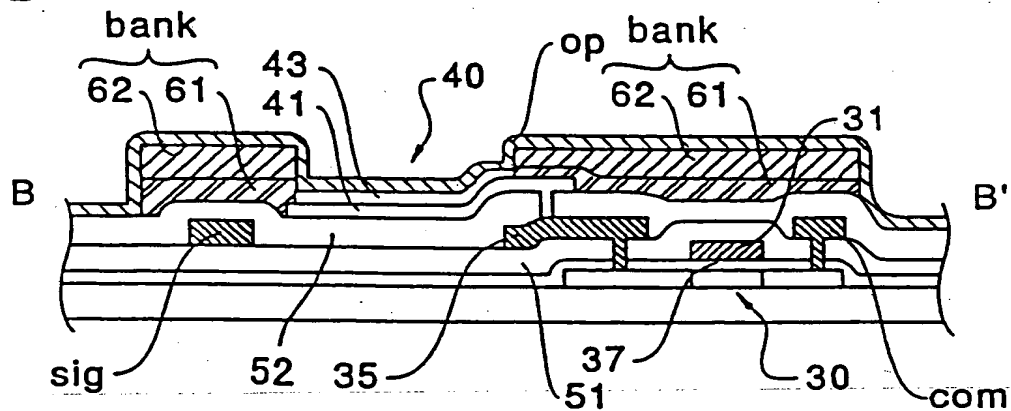


Fig. 18C

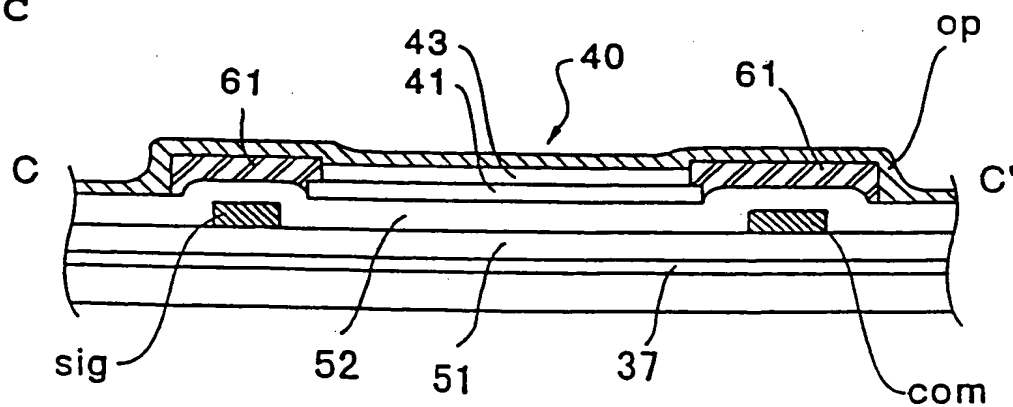


Fig. 19

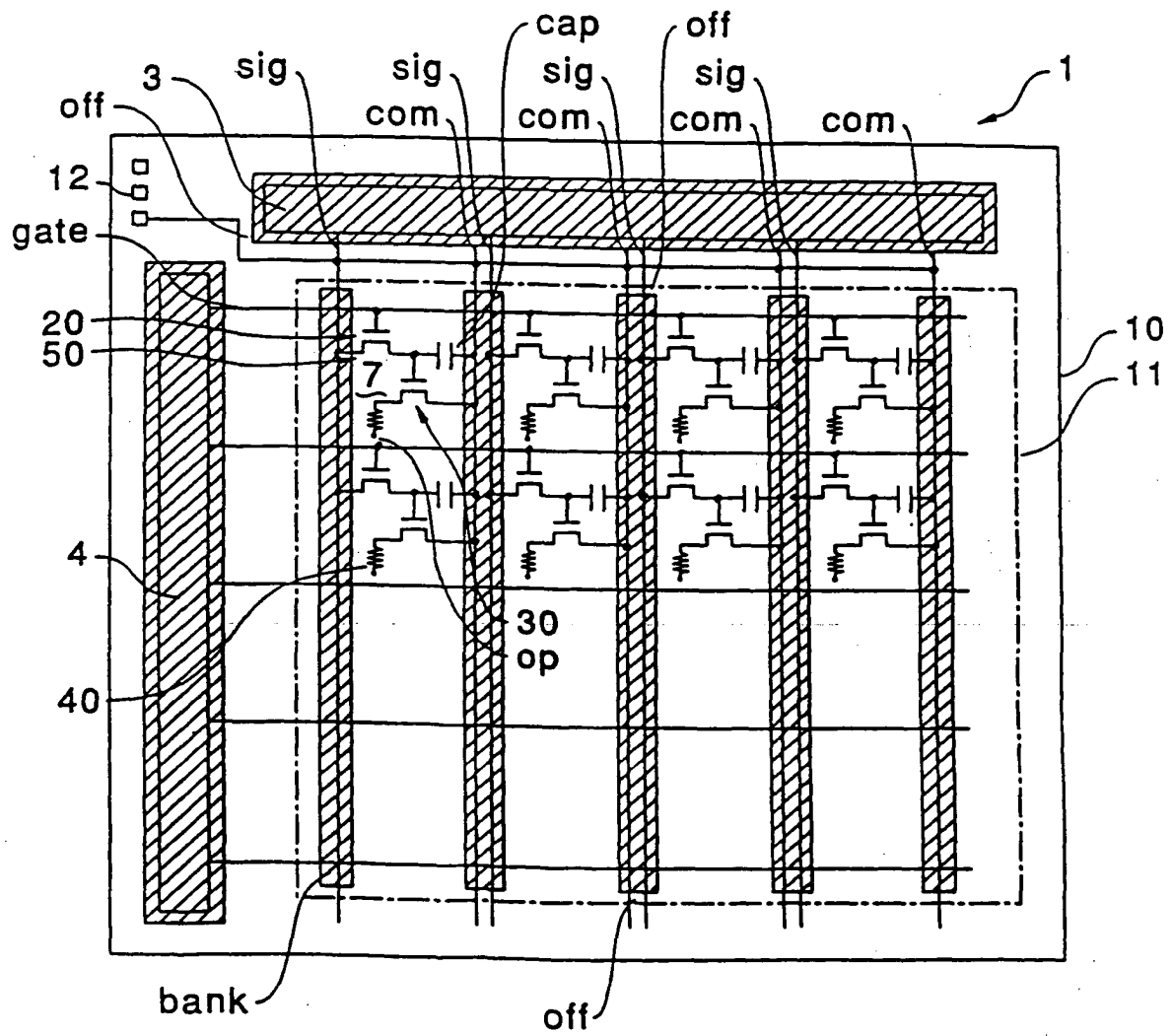


Fig. 20

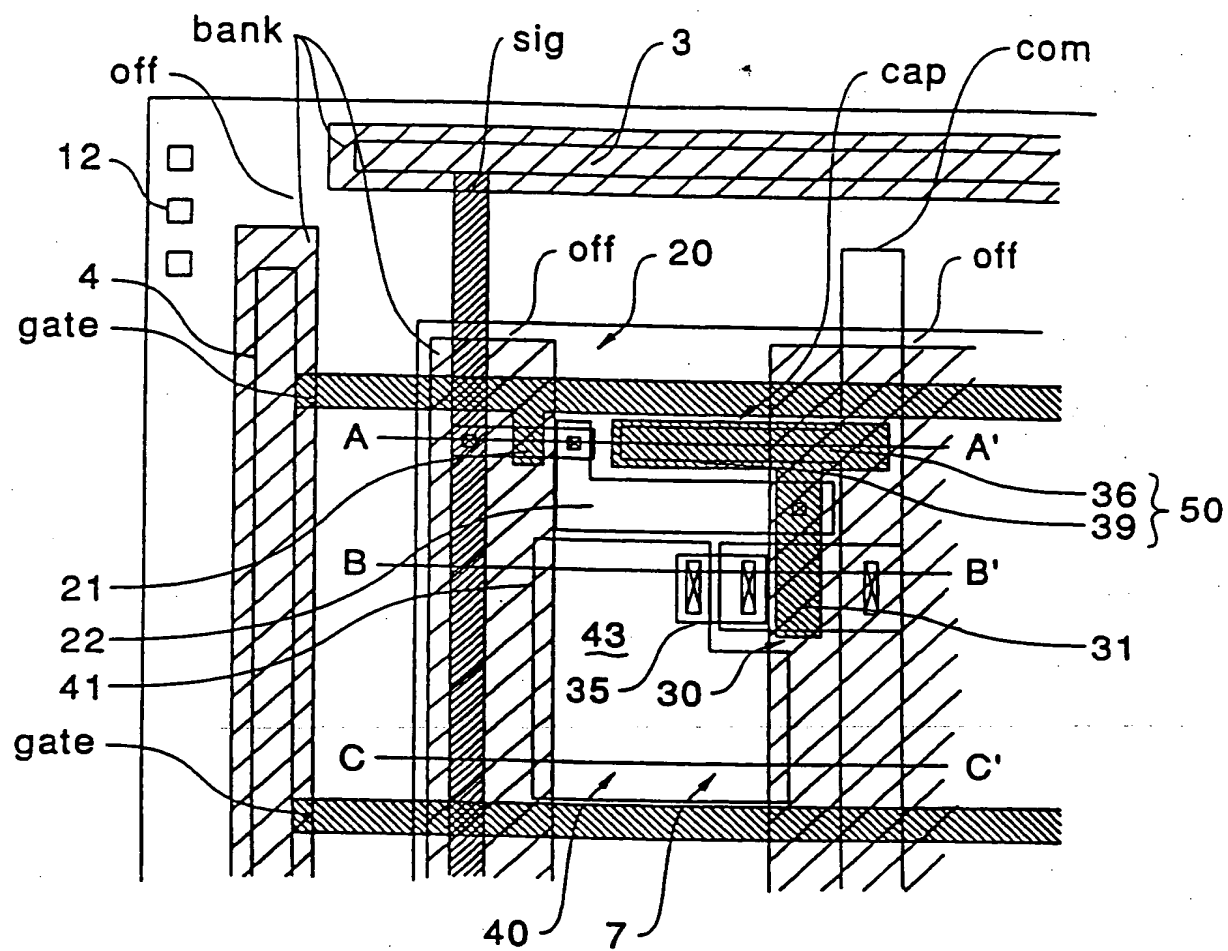


Fig. 21A

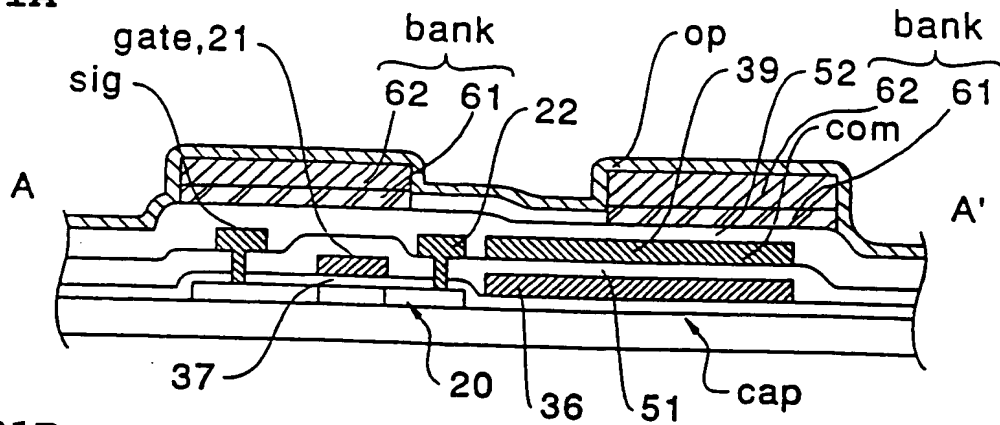


Fig. 21B

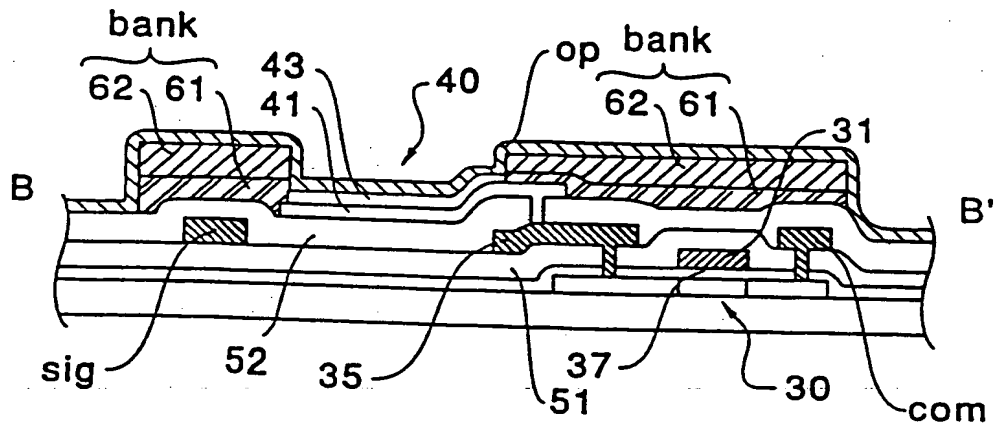


Fig. 21C

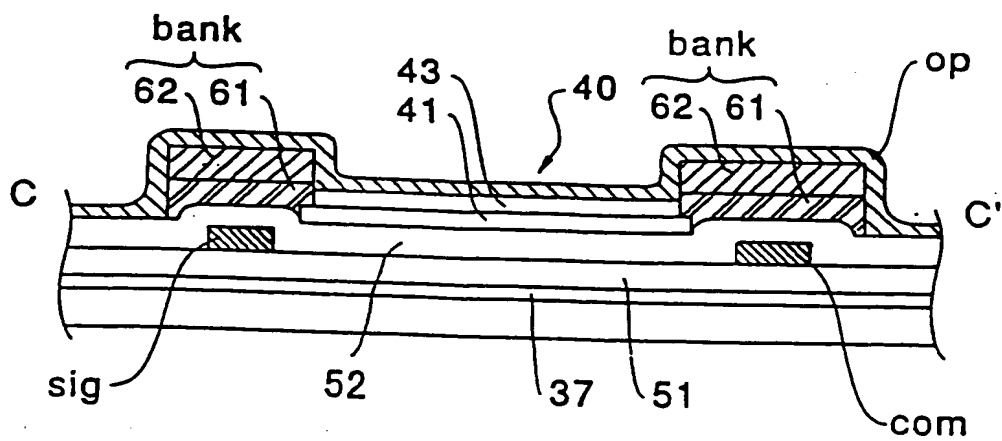


Fig. 22

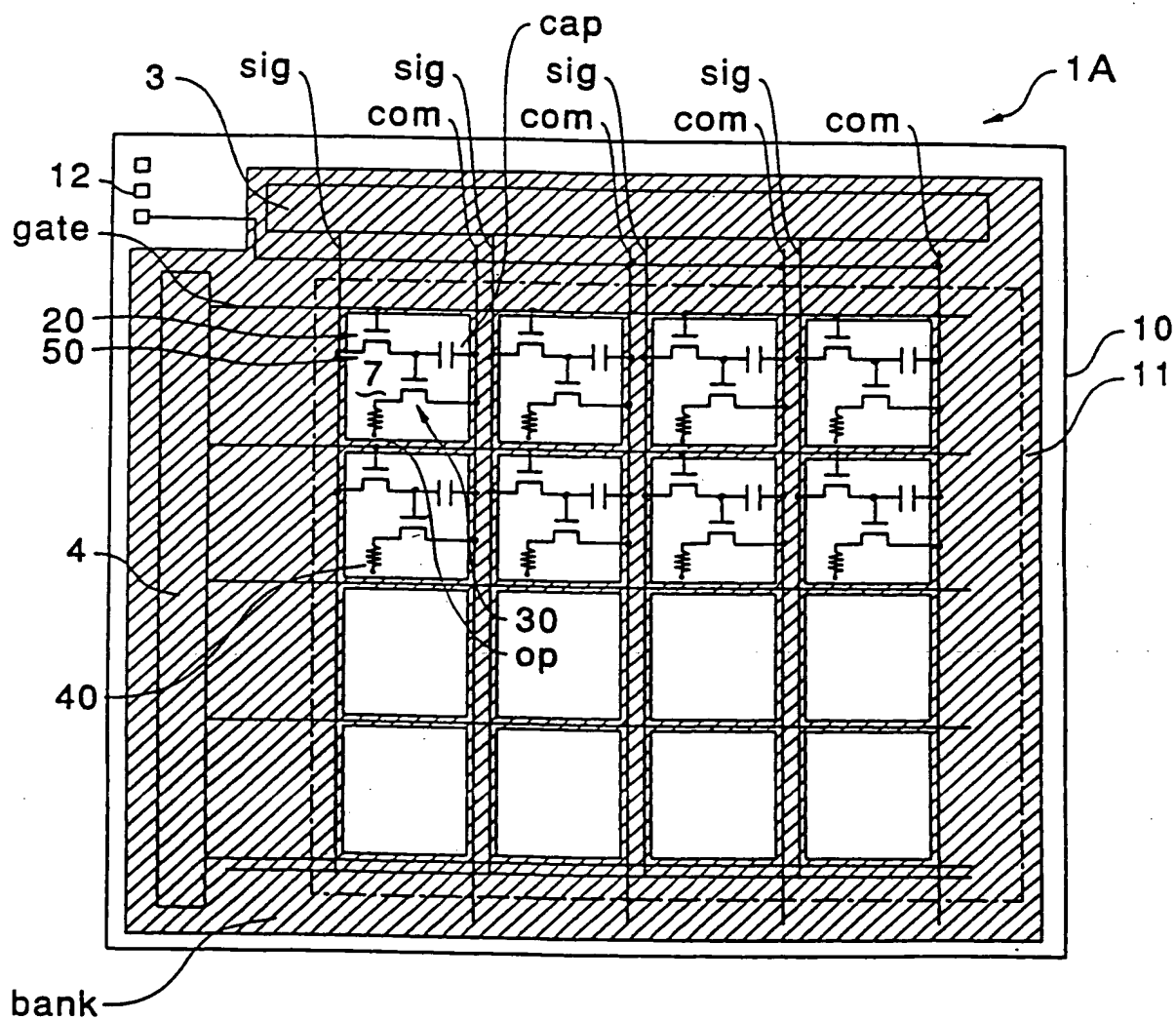


Fig. 23

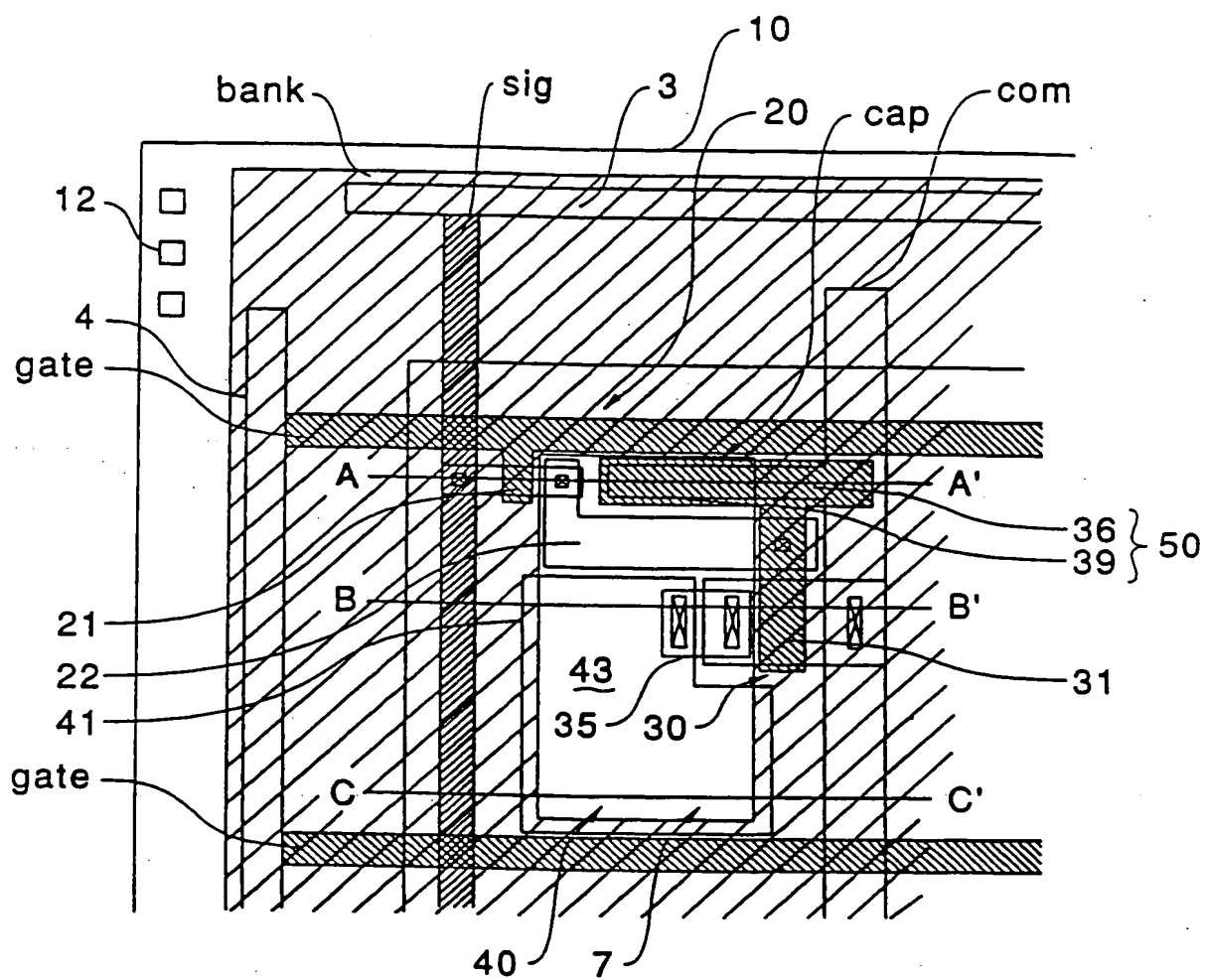


Fig. 24A

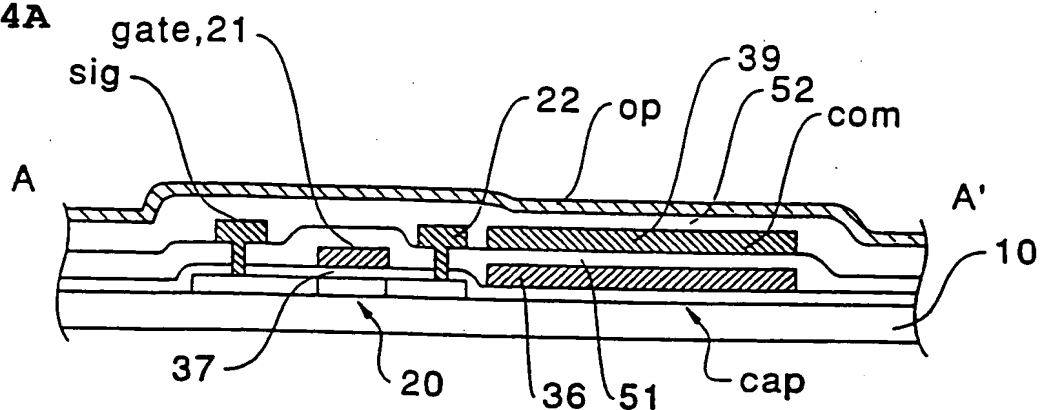


Fig. 24B

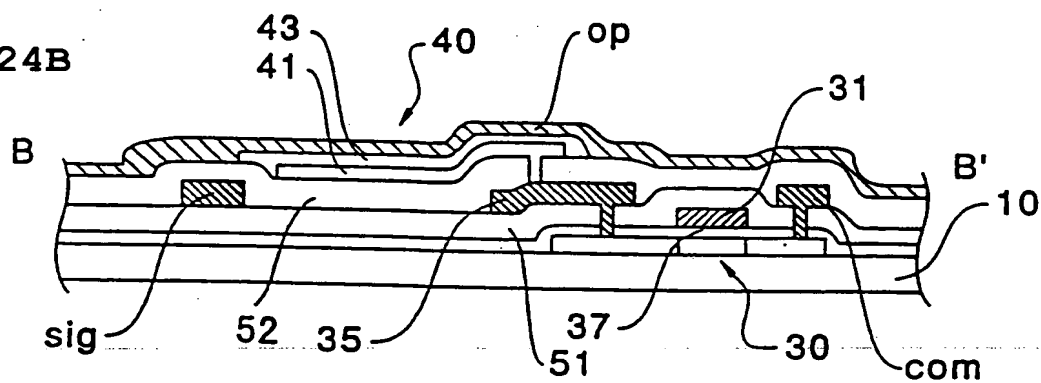


Fig. 24C

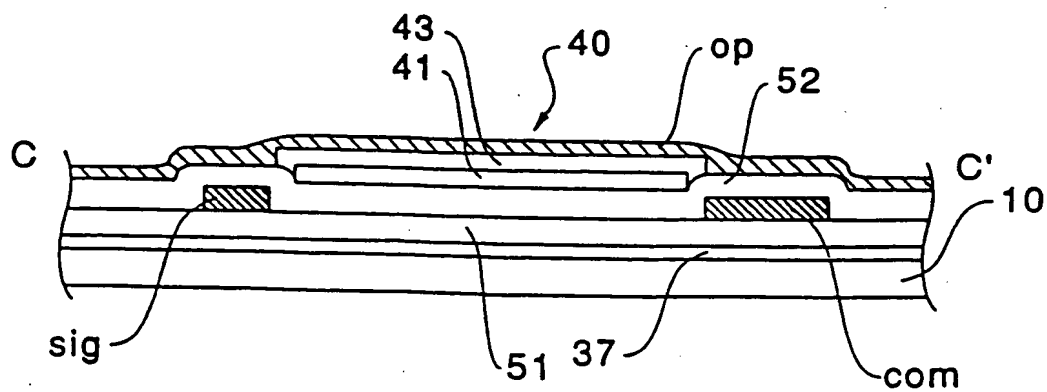


Fig. 25A

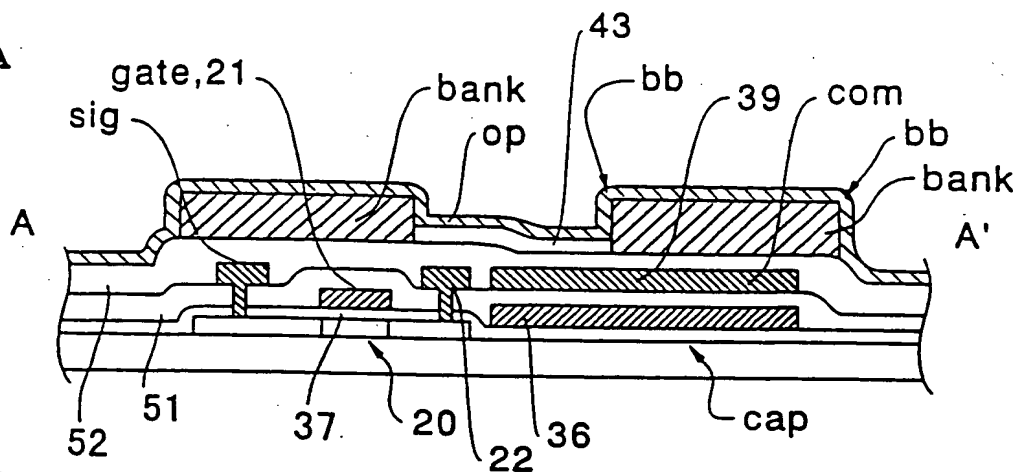


Fig. 25B

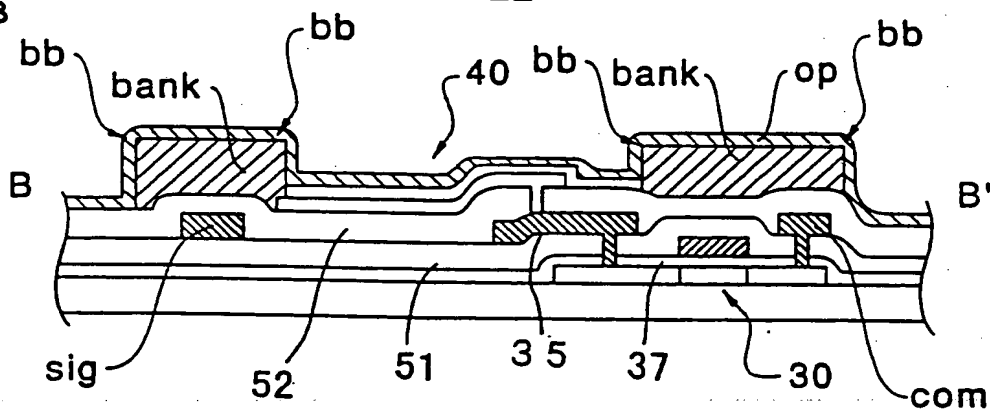


Fig. 25C

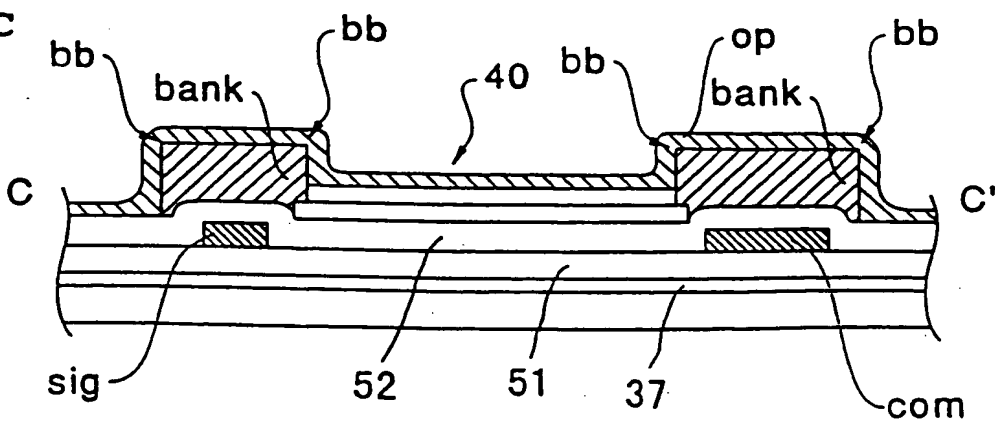


Fig. 26

